Automotive AEC-Q100 Grade 2 Compliance

Reliability Qualification Report

for

DDRIIIL SDRAM with Pb/Halogen Free

(256M×8, 25nm SDRAM AS4C256M8D3LC-12BAN)

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0. RELIABILITY TEST SUMMARY

Test Item	Test Condition	Pass Criteria	Test Result
EFR	1.2*Vint, 125°C, 48Hrs	0 - 1 (Year) ≦1000 (DPM)	0/800 x 3 0 DPM (PASS)
OLT	1.1*Vint, 125°C, 1000Hrs	1 - 10 (Year) ≦50 (FIT)	0/77 x 3 15 FIT (PASS)
			MTBF= 67 x 10^6 Hrs
MSLT	Level III	0/1 (A/R)	0/231 x 3 (PASS)
HTST	150℃, 1000Hrs	0/1 (A/R)	0/45 x 1 (PASS)
TCT	-65℃ ~ +150℃, @3cph, 500Cycles	0/1 (A/R)	0/77 x 3 (PASS)
PCT	121℃, 100%R.H., 2.0atm, 96Hrs	0/1 (A/R)	0/77 x 3 (PASS)
HAST	130℃, 85%R.H., 2.3atm, 1.45V, 96Hrs	0/1 (A/R)	0/77 x 3 (PASS)
ESD	HBM: R=1.5KΩ, C=100pF	≧±2KV	0/3 x 1 (PASS)
	MM: R=0KΩ, C=200pF	≧±200V	0/3 x 1 (PASS)
	CDM: Non-Socket Mode	≧±1KV	0/3 x 1 (PASS)
Latch-Up	Vtr(+)≧1.5 * Vcc Vtr(-)≦-0.5 * Vcc Itr(+)≧100mA Itr(-)≦-100mA		0/6 x 1 (PASS)

Moisture Sensitivity Level Test Flow & Condition:
Electrical Test → SAT → TC (-65℃~+150℃, 5Cycles) → Bake (125℃, 24Hrs) → Soak Level III (30℃, 60%R.H., 192Hrs) → Convection Reflow (260 +5/-0℃, 0~20Secs, 3Cycles) → Electrical Test → SAT

1. INTRODUCTION

In order to meet the most stringent market demands for high quality and reliability semiconductor components, Alliance maintains a strict reliability program in all products. The purpose of this report is to give an overview of the reliability status of AS4C256M8D3LC-12BAN. Accelerated tests are performed on product, and then the re-sults are extrapolated to standard operating conditions in order to calculate and estimate the component’s failure rate.

2. PRODUCT INFORMATION

The AS4C256M8D3LC-12BAN is a 256M*8 bits high-speed CMOS Double Data Rate Three Synchronous Dynamic Random Access Memory (DDRIIIL SDRAM) operat-ing from a single 1.283 to 1.45 Volt power supply. By employing some new CMOS circuit design technologies and the advanced DRAM process technologies, the AS4C256M8D3LC-12BAN is well suited for applications requiring high memory bandwidth and particularly well suited to high performance PC applications. The AS4C256M8D3LC-12BAN is packaged in a standard 78ball, plastic 7.5x10.5mm wBGA.

3. RELIABILITY

Many stress tests have been standardized in such documents as JESD22 and AEC-Q100. From these standards, Alliance has selected a series of tests to en-sure that reliability targets are being met. These tests, including life test, environ-mental test, ESD test and latch-up test, are discussed in the following sections.

According to the qualification family concept from Jedec standard No.47, some of the product or package qualification data can be shared with other similar products that have the same Fab process or Assy construction.

3.1. Sample Preparation Flow

CP → Assembly 78B BGA → FT → Sampling Good Parts for Reliability Test

3.2. Life Test

The purpose of the Early Failure Rate (EFR) is to estimate the infant mortality failure rate that occurs within the first year of normal device operation by accelerating infant mortality failure mechanisms. The oven temperature for the EFR test is 125°C. Testing is performed with dynamic signals applied to the device, and the voltage is 1.2*Vint.

The purpose of the Operating Life Test (OLT) is to determine the reliability of products by accelerating thermally activated failure mechanisms by subjecting samples to extreme temperatures under biased operating condition of 1.1*Vint. The test is used to predict long-term failure rates in terms of FITs (failures in time), with one FIT representing one failure in 10^9 device-hours. The test samples are screened directly after final electrical testing. The oven temperature for the OLT is 125°C. Testing is performed with dynamic signals applied to the device, and the voltage is 1.1*Vint.

3.2.1. Test Flow

(1) EFR Test Flow

B/I 48Hrs (125°C, 1.2*Vint) → Electrical Test (105°C, 25°C, -40°C)

(2) OLT Test Flow

B/I 168Hrs (125°C, 1.1*Vint) → Electrical Test (105°C, 25°C, -40°C)
→ B/I 500Hrs (125°C, 1.1*Vint) → Electrical Test (105°C, 25°C, -40°C)
→ B/I 1000Hrs (125°C, 1.1*Vint) → Electrical Test (105°C, 25°C, -40°C)

3.2.2. Test Criteria

Test Item	Reference Standard	Test Condition	Prediction Duration	Pass Criteria
EFR 48Hrs	AEC Q100-008	Vcc= 1.2*Vint Ta= 125°C	0 – 1 (Year)	≦1000 (DPM)
OLT 1000Hrs	JESD22-A108	Vcc= 1.1*Vint Ta= 125°C	1 – 10 (Year)	≦50 (FIT)

3.2.3. Failure Rate Calculation and Test Result

The life test is performed for the purpose of accelerating the probable electrical and physical weakness of devices subjected to the specified conditions over an extended time period.

By choosing the appropriate thermal activation energy (Ea), data taken at an elevated temperature can be translated to a lower standard operating temperature through the Arrhenius equation:

T(AF)= Exp [(Ea/k)*(1/Tn-1/Ts)]…(1)

where

T(AF)= Temperature Acceleration Factor

Tn= Normal Temperature in Absolute Temperature (K)

Ts= Stress Temperature in Absolute Temperature (K)

k= Boltzmann's Constant (8.62*10^-5 eV/K)

Ea= Thermal Activation Energy

By choosing the appropriate electrical field acceleration rate constant (Vf), data taken at an elevated voltage can be translated to a lower standard operating voltage through the Eyring model:

E(AF)= Exp [Vf*(Vs-Vn)]…(2)

where

E(AF)= Electrical Field Acceleration Factor

Vn= Normal Operating Voltage

Vs= Stress Operating Voltage

Vf= Electrical Field Acceleration Rate Constant

By combining the equation (1) & (2), the failure rate (λ) can be calculated by using the following equation:

λ(FIT)= [(Lamda of 60% CL) / (2*TDH*AF)]*10^9…(3)

where

λ= Failure Rate in FIT

AF= Acceleration Factor

= T(AF) * E(AF)

TDH= Total Device-Hours of the Test

= Device No. * Hour

Lamda of CL= 60% Confidence Level (Refer to the Following Table)

DF	Lamda
1	0.70
2	1.83
3	2.95
4	4.04
5	5.13
6	6.21
7	7.28
8	8.35
9	9.41
10	10.50

DF= 2 * (Failure No. + 1)

Therefore, from equation (3), we can get the FIT number for our OLT experiment. The MTBF can be also calculated from the reciprocal of the FIT rate multiplied by $10^{9.}$

3.2.3.1. EFR Test Result

A summary of Early Failure Rate (EFR) data for the AS4C256M8D3LC-12BAN is listed in Table 1, where the total of 2,400 devices at 125°C has been collected with 0 failure.

Test Item	Sample	Test Result (Failure / Sample Size)	Failure Mode
		48 Hrs	
EFR	2400ea	0/800 x 3 [= 0 DPM]	N/A

Table 1. EFR Test Result for 0-1 Year Prediction

3.2.3.2. OLT Test Result

A summary of Operating Life Test (OLT) data for the AS4C256M8D3LC-12BAN is listed in Table 2, where the total of 231,000 device-hours at 125°C has been collected with 0 failure. We then use Ea= 0.5eV and Vf= 7.0(1/V) (a worse case value from Alliance's foundry) to calculate the failure rate with a 60% confi-dence level. Table 3 shows the final result that the failure rate of 15 FIT at Ta = 55°C and Vcc = 1.35V is predicted.

Test Item	Sample	Test Result (Failure / Sample Size)			Failure Mode
		168 Hrs	500 Hrs	1000 Hrs	
OLT	231ea	0/77 x 3	0/77 x 3	0/77 x 3	N/A

Table 2. OLT Test Result

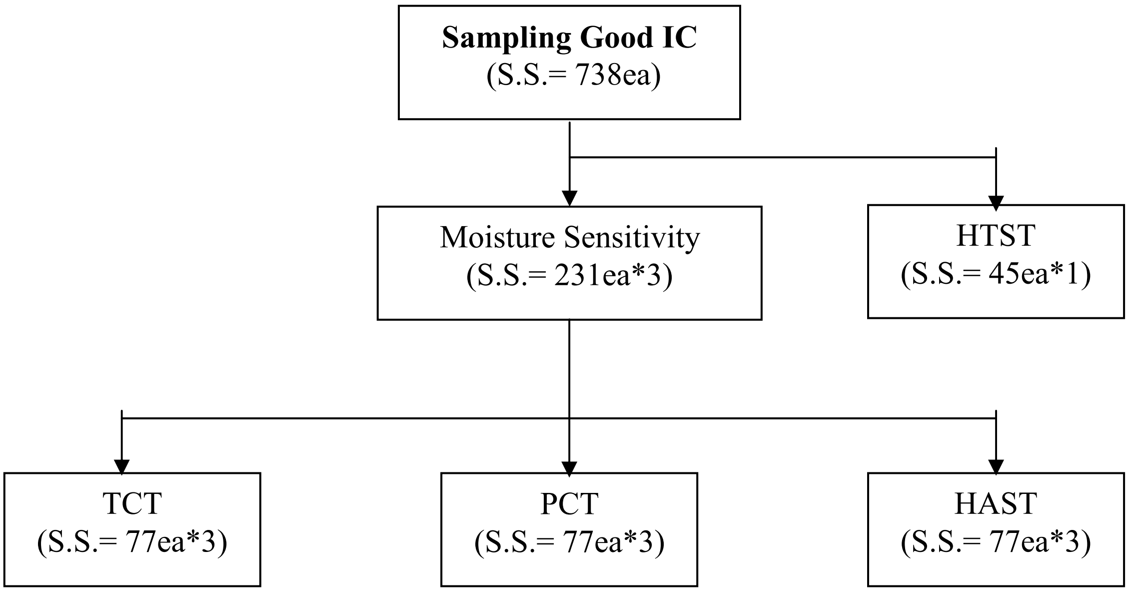
Sample	Device -Hours	Total Failure	Failure Rate Prediction (Ea= 0.5eV, Vf= 7.0(1/V))		
			55°C & 1.35V (% / 1000hrs)	λ (FIT)	MTBF (Hr)
231ea	231,000	0ea	0.0015	15	67×10^6

Table 3. OLT for 1-10 Year Failure Rate Prediction

3.3. Environmental Test

The purpose of environmental test is to evaluate the ability of semicon-ductor device to withstand the temperature stress, humidity stress, electrical stress or any combination of these. It can reveal not only the package quality issue but also the possible error in wafer process or chip design interacting with the assembly process.

3.3.1. Test Flow



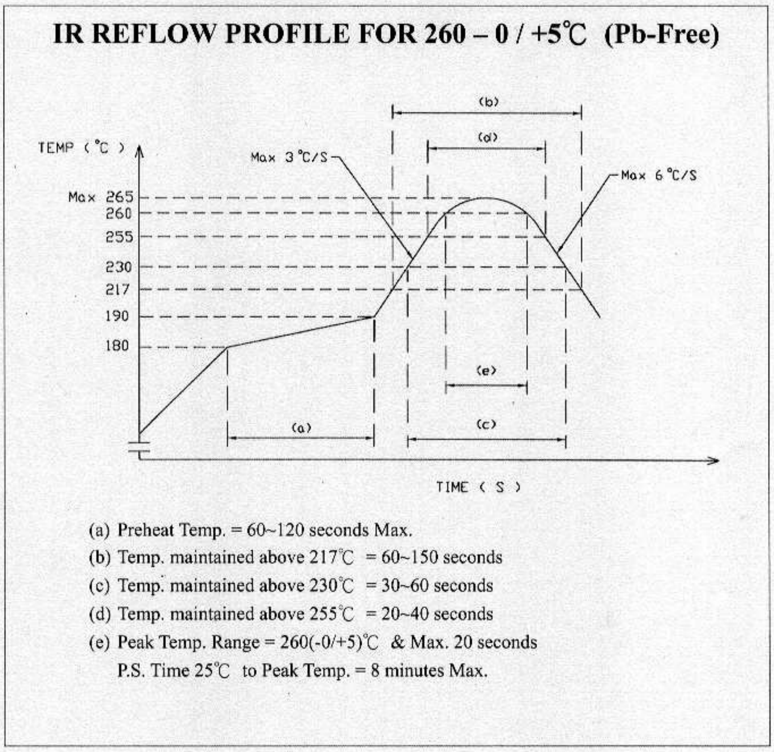
3.3.2. Test Condition and Time

3.3.2.1. Moisture Sensitivity Test

The purpose of moisture sensitivity test is to identify the classification level of nonhermetic solid state Surface Mount Devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid subsequent thermal and mechanical damage during the assembly solder reflow attachment and/or repair operation.

***Moisture Sensitivity Test Flow**

Electrical Test → SAT → TC (-65℃~+150℃, 5Cycles) → Bake (125℃, 24Hrs) → Soak Level III (30℃, 60%R.H., 192Hrs) → Convection Reflow (260 +5/-0℃, 0~20Secs, 3Cycles) → Electrical Test → SAT

Test Item	Test Condition (Level III)	Test Time
Temp. Cycle	-65℃ ~ +150℃	5Cycles
Bake	125℃	24Hrs
Unbiased Temp-Humidity Soak	30℃, 60%R.H.	192Hrs
Convection Reflow		3Cycles

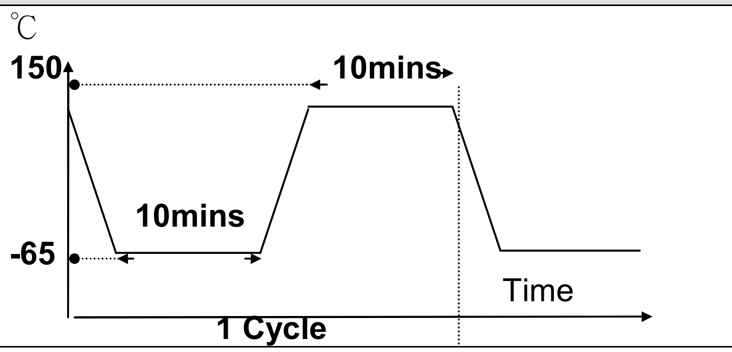
3.3.2.2. High-Temperature Storage Life Test

The high-temperature storage life test measures device resistance to a high-temperature environment that simulates a storage environment. The stress temperature is set to 150℃ in order to accelerate the effect of temperature on the test samples. In the test, no voltage bias is applied to the devices.

Test Item	Test Condition	Test Time
HTST	150℃	1000Hrs

3.3.2.3. Temperature Cycling Test

The purpose of temperature cycling test is to study the effect of thermal expansion mismatch among the different components within a specific die and package system. The cycling test system has a cold dwell at -65℃ and a hot dwell 150℃, and it employs a circulating air environment to ensure rapid stabilization at a specified temperature. During temperature cycling test, devices are inserted into the cycling test system and held at cold dwell for 10 minutes, then the devices are heated to hot dwell for 10 minutes. One cycle includes the duration at both extreme temperatures and the two transition times. The transition period is less than one minute at 25℃. Samples of surface mount devices must first undergo preconditioning and pass a final electrical test prior to the temperature cycling test.

Test Item	Test Condition	Test Time
TCT		500Cycles

3.3.2.4. Pressure Cooker Test

The pressure cooker test is an environmental test that measures device resistance to moisture penetration and the effect of galvanic corrosion. The stress conditions for the pressure cooker are 121℃, 100% relativity humidity, and 2.0atm pressure. Samples of surface mount devices are subjected to preconditioning and a final electrical test prior to the pressure cooker test.

Test Item	Test Condition	Test Time
PCT	121℃, 100%R.H., 2.0atm	96Hrs

3.3.2.5. Highly-Accelerated Temperature and Humidity Stress Test

The highly-accelerated temperature and humidity stress test is performed for the purpose of evaluating the reliability of nonhermetic packaged solid-state device in an environment with high humidity. It employs severe condition of temperature, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductor that pass through it. The stress conditions of the HAST are 130℃, 85% relativity humidity, 2.3atm pressure, and 1.45V maximum operating voltage. Samples of surface mount devices are subjected to preconditioning and a final electrical test prior to the highly-accelerated temperature and humidity stress test.

Test Item	Test Condition	Test Time
HAST	130℃, 85%R.H., 2.3atm, 1.45V	96Hrs

3.3.3. Test Criteria and Result

Table 4 shows the test results and reference standard of environmental test. The test status and results of AS4C256M8D3LC-12BAN are also pre-sented in the table. All pass from these test results mean that Alliance's SDRAM products are much more endurable in most of their service environment.

Test Item	Reference Standard	A/R Criteria	Failure/S.S.	Status	Failure Mode
Moisture Sensitivity	J-STD-020	0/1	0/231 x 3	PASS	N/A
HTST	JESD22-A103	0/1	0/45 x 1	PASS	N/A
TCT*	JESD22-A104	0/1	0/77 x 3	PASS	N/A
PCT*	JESD22-A102	0/1	0/77 x 3	PASS	N/A
HAST*	JESD22-A110	0/1	0/77 x 3	PASS	N/A

*** Sampling from Moisture Sensitivity**

Table 4. Environmental Test Criteria and Result

3.4. ESD Test

Electrical discharge into semiconductor product is one of the leading causes of device failure in the customer‘s manufacturing process. Alliance per-forms the ESD test to ensure that the performance of AS4C256M8D3LC-12BAN will not be degraded to an unacceptable level by exposure to a succession of electro-static discharge. The test methods and test results are shown in Table 5.

Test Item	Test Method				Result (F/S.S)
	Reference Standard	Test Condition	Criteria	Sample	
H.B.M.	AEC Q100-002	R=1.5KΩ, C=100pF	≥±2KV	3ea	0/3
M.M.	AEC Q100-003	R=0KΩ, C=200pF	≥±200V	3ea	0/3
C.D.M.	AEC Q100-011	Non-Socket Mode	≥±1KV	3ea	0/3

Table 5. ESD Test Condition and Result

3.5. Latch-Up Test

CMOS products can be prone to over-voltage exceeding the maximum device rating if the parasitic p-n-p-n SCRs (Silicon-controlled rectifier) are im-properly biased. When the SCR turns on, it draws excessive current and causes products being damaged by thermal runaway. The Table 6 shows the latch-up test method and the test result of no failure.

Test Item	Test Method			Result (F/S.S)
	Reference Standard	Test Condition & Criteria	Sample	
Latch-Up	AEC Q100-004	Vtr(+)≧1.5 * Vcc Vtr(-)≦-0.5 * Vcc Itr(+)≧100mA Itr(-)≦-100mA	6ea	0/6

Table 6. Latch-Up test Condition and Result

4. CONCLUSION

Reliability test is to ensure the ability of a product in order to perform a required function under specific conditions for a certain period of time. Through those tests, the devices of potential failure can be screened out before shipping to the customer. At the same time, the test results are fed back to process, design and other related departments for improving product quality and reliability.

According to the life time test data, *the short-term 48Hrs failure rate (= the normal operation 0-1 year) of* AS4C256M8D3LC-12BAN *is equal to 0 DPM at Ta=55℃ and Vcc=1.35V with 60% confidence level AND the long-term 1000Hrs failure rate (= the normal operation 1-10 year) of* AS4C256M8D3LC-12BAN *is equal to 15 FIT at Ta=55℃ and Vcc=1.35V with 60% confidence level.* The results of environmental test, ESD test and latch-up test also ensure that AS4C256M8D3LC-12BAN is manufactured under a precise control of quality work by Alliance and its subcontractors. ***Thus, this experiment based on the* Alliance *reliability test standard for above test items can all pass*.**

With the extensive research and development activities and the cooperation of all departments, Alliance continuously sets and maintains higher standard of quality and reliability to satisfy the future demand of its customers.